2665

Form: PTO/SB/17 (Modified)

OIPE SEP 04 2003 PATENT & TRADEMARK OFFICE

REPLY/AMENDMENT FEE TRANSMITTAL

Attorney Docket No.	95-333
Application Number	09/496,212
Filing Date	Febraury 1, 2000
First Named Inventor	VISWANATH et al.
Group Art Unit	2665
Examiner Name	RYMAN, Daniel J.

AMOUNT ENCLOSED	$ 0

FEE CALCULATION (fees effective 10/01/2001)

CLAIMS AS AMENDED	Claims Remaining After Amendment	Highest Number Previously Paid For	Number Extra	Rate	Calculations
TOTAL CLAIMS	18	20	0 (3)	X $18.00 =	$0
INDEPENDENT CLAIMS	3	3	0	X $84.00 =	$0

Since an Official Action set an original due date of____, petition is hereby made for an extension to cover the date this reply is filed for which the requisite fee is enclosed (1 month ($110); 2 months ($400); 3 months ($920); 4 months ($1,440); 5 months ($1,960)):	
If Statutory Disclaimer under Rule 20(d) is enclosed, add fee ($110)	+
Total of above Calculations =	$0
Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28)	-
TOTAL FEES DUE =	$0

(1) If entry (1) is less than entry (2), entry (3) is "0".
(2) If entry (2) is less than 20, change entry (2) to "20".
(4) If entry (4) is less than entry (5), entry (6) is "0".
(5) If entry (5) is less than 3, change entry (5) to "3".

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METHOD OF PAYMENT

[ ] Check enclosed as payment.

[ ] Charge "TOTAL FEES DUE" to the Deposit Account No., below.

AUTHORIZATION

[X] If the above-noted "AMOUNT ENCLOSED" is not correct, the Commissioner is hereby authorized to credit any overpayment or charge any additional fees under 37 CFR 1.16 or 1.17 necessary to maintain pendency of the present application to:

Deposit Account No.:	50-0687
OrderNo.: (Client/Matter)	95-333

SUBMITTED BY: MANELLI DENISON & SELTER PLLC

Typed Name	Leon R. Turkevich	Reg. No.	34,035
Signature	L R T	Date	September 4, 2003

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9-23-03

Docket No.: 95-333 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
VISWANATH et al.	:	
Serial No.: 09/496,212	:	Group Art Unit: 2665
Filed: February 1, 2000	:	Examiner: Ryman, Daniel J.

For: ARRANGEMENT FOR SEARCHING PACKET POLICIES USING MULTI-KEY HASH SEARCHES IN A NETWORK SWITCH

RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Official Action mailed June 9, 2003, Applicant hereby submits the following remarks.

Reconsideration and allowance of the above-referenced application are respectfully requested. Claims 1-3 and 5-19 are unchanged and remain pending in the application.

Acknowledgement of the formal drawings submitted April 16, 2001 and the Drawing Change Authorization Request submitted April 29, 2003 is respectfully requested.

Claims 1-3, 5-8 and 11-13 stand rejected under §103 in view of U.S. Patent No. 5,852,607 to Chin in view of U.S. Patent No. 5,949,786 to Bellenger. This rejection is respectfully traversed.

As admitted in the Official Action, Chin does not disclose a table configured for storing layer 3 switching entries. Further, Chin does not disclose a table configured for storing layer 3 signatures, as claimed.

Moreover, Chin does not disclose generating first and second hash keys as suggested in the Official Action, let alone where the first and second hash keys are combined into a signature for the received packet. Rather, Chin discloses at col. 6, lines 1-42 that only the 48-bit MAC address contained in the destination address field is hashed into a 12-bit hash value "I" by the hash circuit; the 12-bit hash value "I" is then combined with a 10-bit VLAN identifier (in the layer 2 header) to form a 12-bit index "J" for accessing the table control circuitry 24.

Finally, Chin neither discloses nor suggests generating the first and second hash keys from respective first and second layer 3 information, as specified in claims 1 and 11. Rather, Chin merely combines layer 2 VLAN information with a hash value of a (layer 2) destination MAC address.

Although Bellenger discloses the hashing of layer 3 information, Bellenger neither discloses nor suggests combining the first and second hash keys (generated from respective first and second layer 3 information), as specified in claims 1 and 12. Rather, Bellenger teaches in Fig. 4 that a certain fields are selected for input to a hash generator 414, resulting in a single hash key (col. 5, lines 52-57). In addition, Fig. 5 shows that only one hash value is selected (based on a flow select 501) for accessing a route table (col. 6, lines 21-32).

Hence, the Official Action fails to establish a prima facie case of obviousness, since neither Chin nor Bellenger, singly or in combination, disclose or suggest the feature of combining the first and second hash keys into a signature for the received data packet.

Further, neither Chin nor Bellenger disclose, singly or in combination, that that packet signatures are generated by a network port of an integrated network switch having a plurality of switch ports as specified in claim 11. Rather, Chin discloses multiple packet processors that are discrete components. Bellenger discloses an integrated network switch 100 with a centralized hash

generator 105. One skilled in the art would avoiding implemeting the system of Chin as a single integrated device, since the manufacture of the switching link 105 with multiple redundant processors 210 having the tables 320 would have been unfeasable due to exhorbitant costs. Applicant notes that the Official Action admits on page 7 (paragraph 14) that the hypothetical combination of Chin and Bellenger does not disclose that the network switch is an integrated circuit chip; hence, this rejection of claim 11 should be withdrawn.

Applicant strenously traverses the assertion that Chin or Bellenger disclose or suggest selecting TCP or UDP information for hashing, as specified in claims 3, 12, and 13: nothing in either of these references provides any suggestion of using TCP or UDP information for hashing, as claimed: Col. 3, lines 6-24 of Chin describe use of VLAN, which is an Ethernet (layer 2) field defined by IEEE 802.3ac and IEEE 802.1Q as a 4-byte field inserted between the original Ethernet frame's Source Address field and Type/Length field; col. 1, lines 42-59 of Bellenger merely provides a general comparison of layer 2 (link layer) addressing versus layer 3 (network layer) protocols, but neither discloses nor suggests using TCP or UDP information for hashing, as claimed.

For these and other reasons, claims 1-3, 5-8, and 11-13 are patentable over Chin and Bellenger. Hence, this rejection should be withdrawn.

Claim 9 stands rejected under §103 in view of Chin, Bellenger, and U.S. Patent No. 5,757,795 to Schnell. This rejection is respectfully traversed.

As described above, one skilled in the art would not have been motivated to implement Chin as a single integrated circuit chip due to the resulting exhorbitant costs due to the substantially large size requirements caused by the redundant processors 210 (in addition to the system processor 215) in Figure 2 of Chin. Schnell merely describes that a layer 2 (Ethernet) switch may be implemented

as an ASIC. However, the "mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

Hence, the rejection of claim 9 should be withdrawn.

Claim 10 is rejected under §103 in view of Chin, Bellenger, U.S. Patent No. 6,157,641 to Wilford and U.S. Patent No. 6,212,183 to Wilford. This rejection is respectfully traversed. At the outset, the rejection fails to identify why one skilled in the art would have been motivated to add the teachings of Wilford ('641) plus Wilford ('183). Regardless, the rejection fails to address the claimed feature of forwarding an identifier specifying the selected layer 3 switching entry from the network switch port having received the received data packet to layer 3 switching logic.

Further, the tortured interpretation of "switching logic" as "memory" is unreasonable: logic is an implementation of boolean algebra, and "memory" is a storage device. Moreover, the tortured interpretation is inconsistent with the specification, which describes that the generating, combining, searching, and forwarding steps are performed in the network switch port, enabling distributed processing that minimizes processing requirements for the layer 3 switching logic in order to provide real-time switching. Hence, "claims are not to be read in a vacuum, and limitations therein are to be interpreted in light of the specification in giving them their 'broadest reasonable interpretation.'" MPEP § 2111.01 at 2100-37 (Rev. 1, Feb. 2000) (quoting In re Marosi, 218 USPQ 289, 292 (Fed. Cir. 1983)(emphasis in original)).

Finally, the argument that a hash key is generated "only once" is nonsensical and inconsistent with the teachings of the applied references: a hash key is generated for each received packet to

determine the corresponding switching entry. For these and other reasons, the rejection of claim 10 should be withdrawn.

Claims 14-19 stand rejected under §103 in view of Chin, Bellenger, and U.S. Patent No. 6,473,400 to Manning. This rejection is respectfully traversed.

As described above, Chin does not disclose an integrated network switch, as claimed. Further, Chin and Bellenger and Manning neither disclose nor suggest generating a packet signature by generating first and second hash keys, as claimed.

Further, Manning provides no disclosure of suggestion of an index table that includes addresses of layer 3 switching entries: the cited portion refers to generating hashed addresses for packet history tables that accumulate statistics for monitored traffic flows (see, e.g., col. 4, line 47 to col. 5, line 65). Manning stresses that it is directed to remote monitoring, and not switching:

> The general form of the switch is not important to the present invention provided that, as will be apparent, the switch has some suitable means for monitoring traffic flow according to "layer 2" conversations and means for sampling packets to provide sampled traffic flow data based on a combination of layer 2 and layer 3 addresses. It is already been remarked that although it is theoretically possible to obtain measures of traffic flow by monitoring all packets and establishing data tables according to every address combination (using both layer 2 and layer 3 addresses), such a process would require excessive computational effort and storage capacity.
>
> (Col. 3, lines 13-25).

Manning is non-analogous art: Manning is directed to gathering remote monitoring (RMON) statistics regarding traffic flow based on sampling data packets, and is not within the field of the inventors' endeavor, namely providing wire-rate layer-2/layer 3 switching of data packets in a non-blocking network switch; further, Manning is not reasonably pertinent to the particular problem with which the inventors were involved, namely providing a non-blocking

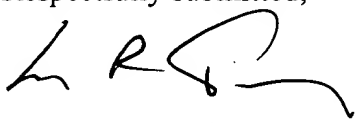
network switch providing layer 3 processing with minimal buffering and latency. Manning provides no disclosure or suggestion of hashed values to identify switching entries, and as such is non-analogous art. In re Wood, 202 USPQ 171, 174 (CCPA 1979).

For these and other reasons, the rejection of claims 14-19 should be withdrawn.

In view of the above, it is believed this application is in condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-333, and please credit any excess fees to such deposit account.

Respectfully submitted,



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Date: September 4, 2003